

Module Handbook (<https://modhb.uni-kl.de/>)

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Module EIT-EMS-657-M-7

Synthesis and Optimization of Microelectronic Systems I (M, 4.0 LP)

Module Identification

Module Number	Module Name	CP (Effort)
EIT-EMS-657-M-7	<i>Synthesis and Optimization of Microelectronic Systems I</i>	4.0 CP (120 h)

Basedata

CP, Effort	4.0 CP = 120 h
Position of the semester	1 Sem. in WiSe
Level	[7] Master (Advanced)
Language	[EN] English
Module Manager	Wehn, Norbert, Prof. Dr.-Ing. (PROF DEPT: EIT) (/staff/349/)
Lecturers	Wehn, Norbert, Prof. Dr.-Ing. (PROF DEPT: EIT) (/staff/349/)
Area of study	[EIT-EMS] Microelectronic Systems Design
Reference course of study	[EIT-88.781-SG#2010] M.Sc. Electrical and Computer Engineering [2010] (/mhb/FB-EIT/cos-556/)
Lifecycle-State	[NORM] Active

Courses

Type/SWS	Course Number	Choice in Module-Part	SL	PL	CP	Sem.
2V+1U	EIT-EMS-657-K-7 (/mhb/courses/EIT-EMS-657-K-7/)	P	-	PL1	4.0	WiSe

- About [EIT-EMS-657-K-7]: Title: "Synthesis and Optimization of Microelectronic Systems I"; Presence-Time: 42 h; Self-Study: 78 h

Examination achievement PL1

- Form of examination: **written exam (Klausur) (60 Min.)**
- Examination Frequency: each semester

Evaluation of grades

The grade of the module examination is also the module grade.

Contents

From [EIT-EMS-657-K-7] **Synthesis and Optimization of Microelectronic Systems I** (/mhb/courses/EIT-EMS-657-K-7/):

- System modeling and specification
- HW/SW Codesign methodologies
- Implementation platforms
- Partitioning
- Discrete optimization techniques e.g. simulated annealing, ILP
- High-Level Synthesis, scheduling, allocation, binding
- RT-synthesis, retiming

Competencies / intended learning achievements

After completing this module you can...

- ... explain and analyze and apply advanced methodologies for the hardware design of embedded systems.
- ... explain, apply and analyze the corresponding algorithms in the design methodology.
- ... explain and apply discrete optimization techniques.
- ... read, summarize. and assess scientific publications in this field.

Requirements for attendance (informal)

Modules:

- [EIT-EIS-571-M-4] Architecture of Digital Systems I (M, 4.0 LP) (/mhb/modules/EIT-EIS-571-M-4/)

Requirements for attendance (formal)

None

References to Module / Module Number [EIT-EMS-657-M-7]

Course of Study	Section	Choice/Obligation
[EIT-88.781-SG#2010] M.Sc. Electrical and Computer Engineering [2010] (/mhb/FB-EIT/cos-556/)	Theoretical Part	[P] Compulsory
[EIT-88.781-SG#2010] M.Sc. Electrical and Computer Engineering [2010] (/mhb/FB-EIT/cos-556/)	Specialization Modules	[P] Compulsory
[EIT-88.?-SG#2021] M.Sc. Electrical and Computer Engineering [2021] (/mhb/FB-EIT/cos-686/)	Major Embedded Systems (ESY)	[P] Compulsory
[EIT-88.A20-SG#2021] M.Sc. European Master in Embedded Computing Systems (EMECS) [2021] (/mhb/FB-EIT/cos-566/)	Core Subjects	[WP] Compulsory Elective
[EIT-88.A20-SG#2021] M.Sc. European Master in Embedded Computing Systems (EMECS) [2021] (/mhb/FB-EIT/cos-566/)	Elective Subjects	[W] Elective Module
[EIT-88.?-SG#2021] M.Sc. Embedded Computing Systems (ESY) [2021] (/mhb/FB-EIT/cos-677/)	Core Program	[WP] Compulsory Elective
[EIT-88.?-SG#2021] M.Sc. Embedded Computing Systems (ESY) [2021] (/mhb/FB-EIT/cos-677/)	Elective Subjects	[W] Elective Module
Module-Pool	Name	
[GS-CVT-EE-E-MPOOL-6 (/mhb/modulepools/GS-CVT-EE-E-MPOOL-6/)]	Catalog Electives Electrical and Computer Engineering	