

Module Handbook (<https://modhb.uni-kl.de/>)

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Course EIT-EIS-660-K-7

Synthesis and Optimization of Microelectronic Systems II (2V, 3.0 LP)

Course Type

| SWS | Type | Course Form | CP (Effort) | Presence-Time / Self-Study | |
|------|------|-------------|-------------|----------------------------|------|
| 2 | V | Lecture | 3.0 CP | 28 h | 62 h |
| (2V) | | | 3.0 CP | 28 h | 62 h |

Basedata

| | |
|--------------------------|---|
| SWS | 2V |
| CP, Effort | 3.0 CP = 90 h |
| Position of the semester | 1 Sem. in SuSe |
| Level | [7] Master (Advanced) |
| Language | [EN] English |
| Lecturers | Kunz, Wolfgang, Prof. Dr.-Ing. (PROF DEPT: EIT) (/staff/344/) |
| Area of study | [EIT-EIS] Electronic Design Automatization |
| Lifecycle-State | [NORM] Active |

Contents

- Synthesis problem at the register transfer level
- Two-level minimization, ESPRESSO
- Functional decomposition
- Boolean and algebraic methods based on division
- Timing analysis
- Technology mapping
- Layout-driven synthesis

Literature

- S. Devadas, A. Ghosh, K. Keutzer: Logic Synthesis. McGraw-Hill, 1994, ISBN 0-07-016500-9.
- G. De Micheli: Synthesis and Optimization of Digital Circuits. McGraw-Hill, 1994, ISBN 0-07-016333-2.

- G. Hachtel, F. Somenzi: Logic Synthesis and Verification Algorithms. Kluwer Academic Publishers, 1996, ISBN 0-7923-9746-0.
- S. Hassoun, T. Sasao: Logic Synthesis and Verification. Kluwer Academic Publishers, 2002, ISBN 0-7923-7606-4.

Materials

- Lecture slides

Requirements for attendance (informal)

Modules:

- [EIT-EIS-571-M-4] Architecture of Digital Systems I (M, 4.0 LP) (/mhb/modules/EIT-EIS-571-M-4/)

Requirements for attendance (formal)

None

References to Course [EIT-EIS-660-K-7]

| Module | Name | Context |
|---|--|-----------------------------|
| [EIT-EIS-660-M-7 (/mhb/modules/EIT-EIS-660-M-7/)] | Synthesis and Optimization of Microelectronic Systems II | P: 2V, 3.0 Obligatory LP |